This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims

1-3. (Cancelled)

4. (Previously presented) The circuit of claim 31, wherein one of the sets of conductive address lines is a plurality of generally parallel doped regions within a semiconductor material.

5. (Previously presented) The circuit of claim 31, wherein one of the sets of conductive address lines is a plurality of generally parallel metalized regions.

6. (Previously presented) The circuit of claim 31, wherein said addressing circuitry comprises circuitry to sequentially select storage locations.

7. (Previously presented) The circuit of claim 31, wherein said addressing circuitry comprises circuitry to randomly select storage locations.

8. (Previously presented) The circuit of claim 31, further comprising display means for displaying alphanumeric or graphic information to a user.

9. (Previously presented) The circuit of claim 31, further comprising input means to enable its user to alter its operation.

10. (Previously presented) The circuit of claim 31, wherein part or all of said circuit is removable or replaceable.

11. (Previously presented) The circuit of claim 31, wherein output from the circuit is in a digital format.

12. (Previously presented) The circuit of claim 31, wherein output from the circuit is in an analog format.

13. (Previously presented) The circuit of claim 31, wherein output from the circuit is in either a digital format or an analog format.

14. – 17. (Cancelled)

18. (Previously presented) The circuit of claim 5, wherein said nonlinear elements are of the metal-on-semiconductor junction type.

19. (Previously presented) The circuit of claim 5, wherein said nonlinear elements are of the p-n junction type.

20. (Cancelled)

21. (Currently amended) The circuit of claim 31, wherein said nonlinear elements[[are]] comprise[[d]] ~~by a transistor as the~~ base-emitter junctions of transistors.

22. (Previously presented) The circuit of claim 31, further comprising means for retaining the address of the information to be accessed.

23. (Previously presented) The circuit of claim 22, further comprising means for incrementing the retained address.

24. (Previously presented) The circuit of claim 22, further comprising means for setting the retained address.

25. – 30. (Cancelled)

31. (Currently amended) An information-storage circuit, the circuit comprising:

a. first and second sets of conductive address lines overlapping with each other and defining storage locations at overlap regions;

b. a series of information-defining nonlinear elements bridging the address lines at least at some of the overlap regions, presence or absence of a nonlinear element at a storage location defining a bit state at the location; and

c. address circuitry for disabling all but a selected one of the first set of address lines, wherein the address circuitry comprises a first pattern of rectifiers directly connected to the first set of address lines.

32. (Currently amended) The circuit of claim 31 further comprising sensing circuitry for sensing the presence or absence of an ~~nonlinear~~ information-defining nonlinear element bridging the selected first-set address line and at least a selected one of the second set of address lines to thereby determine the bit state at each storage location defined by selected address lines.

33. (Previously presented) The circuit of claim 31 wherein the all but one of the first set of address lines is disabled by shifting a voltage thereon.

34. (Previously presented) The circuit of claim 31 further comprising additional address circuitry for disabling all but a selected one of the second set of address lines.

35. (Previously presented) The circuit of claim 34 wherein the all but one of the second set of address lines is disabled by shifting a voltage thereon.

36. (Previously presented) The circuit of claim 34 wherein:

a. the information-defining nonlinear elements have a threshold activation voltage associated therewith;

b. the address circuitry comprises circuitry for setting all but the selected one of the first set of address lines to a first voltage level; and

c. the additional address circuitry comprises circuitry for setting all but the selected one of the second set of address lines to a second voltage level, the first and second voltage levels differing by at least the threshold activation voltage.

37. (Currently amended) The circuit of claim 36 wherein:

a. the address circuitry further comprises a first set of selectable disabling lines fewer in number than and connected to the first set of address lines by [[a]]the first pattern of ~~nonlinear elements~~rectifiers, and circuitry for applying a third voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of address lines; and

b. the additional address circuitry further comprises a second set of selectable disabling lines fewer in number than and connected to the second set of address lines by a second pattern

of nonlinear elements, and circuitry for applying a fourth voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of address lines.

38. (Previously presented) The circuit of claim 37 wherein the third voltage is substantially equal to the second voltage and the fourth voltage is substantially equal to the first voltage.

39. (Currently amended) The circuit of claim 38 wherein all of the nonlinear elements have [[a]]said threshold activation voltage associated therewith, application of the threshold activation voltage across the nonlinear elements allowing current to flow therethrough.

40. (Previously presented) The circuit of claim 36 wherein the information-defining nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop so that an information-defining rectifier, if present at the storage location defined by the selected address lines, is forward biased.

41. (Previously presented) The circuit of claim 39 wherein all of the nonlinear elements are rectifiers having an associated voltage drop corresponding to the threshold activation voltage, the first and second voltages differing by at least the rectifier voltage drop.

42. (Currently amended) The circuit of claim 36 wherein the second voltage is approximately a ground voltage~~or near to ground~~.

43. (Cancelled)

44. (Previously presented) The circuit of claim 32 wherein the sensing circuitry is configured to sense current when an information-defining nonlinear element is not present at the storage location of the selected first-set address line and a selected second-set conductive address line.

45. (Previously presented) The circuit of claim 44 wherein the sensing circuitry comprises an output line connected to each of the first set of address lines by a sensing nonlinear element.

46. (Currently amended) The circuit of claim 45 wherein the address circuitry comprises a first set of selectable disabling lines fewer in number than and connected to the first set of address lines by [[a]]the first pattern of ~~nonlinear elements~~rectifiers, and circuitry for applying a second voltage to at least some of the first set of disabling lines to thereby disable all but one of the first set of address lines, the information-storage circuit further comprising additional address circuitry which itself comprises (i) a second set of selectable disabling lines fewer in number than and connected to the second set of address lines by a second pattern of nonlinear elements, and (ii) circuitry for applying a first voltage to at least some of the second set of disabling lines to thereby disable all but one of the second set of address lines, all of the nonlinear elements having a threshold activation voltage associated therewith, application of the threshold activation voltage across the nonlinear elements allowing current to flow therethrough.

47. – 50. (Cancelled)

51. (Previously presented) The circuit of claim 31 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

52. (Previously presented) The circuit of claim 51 wherein the first and second series of voltage drop elements are resistors.

53. (Previously presented) The circuit of claim 51 wherein the first and second series of voltage drop elements are nonlinear elements.

54. (Previously presented) The circuit of claim 53 wherein the nonlinear elements are rectifiers.

55. (Previously presented) The circuit of claim 54 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

56. (Currently amended) The circuit of claim 51 wherein the second voltage is approximately a ground voltage~~or near to ground~~.

57. (Previously presented) The circuit of claim 32 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

58. (Previously presented) The circuit of claim 57 wherein the first and second series of voltage drop elements are resistors.

59. (Previously presented) The circuit of claim 57 wherein the first and second series of voltage drop elements are nonlinear elements.

60. (Previously presented) The circuit of claim 59 wherein the nonlinear elements are rectifiers.

61. (Currently amended) The circuit of claim 60[[1]] further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

62. (Currently amended) The circuit of claim 57 wherein the second voltage is approximately a ground voltage~~or near to ground~~.

63. (Previously presented) The circuit of claim 46 further comprising a first series of voltage-drop elements connecting the first set of address lines to circuitry for applying a first voltage and a second series of voltage drop elements connecting the second set of address lines to a circuitry for applying a second voltage.

64. (Previously presented) The circuit of claim 63 wherein the first and second series of voltage drop elements are resistors.

65. (Previously presented) The circuit of claim 63 wherein the first and second series of voltage drop elements are nonlinear elements.

66. (Previously presented) The circuit of claim 65 wherein the nonlinear elements are rectifiers.

67. (Previously presented) The circuit of claim 66 further comprising circuitry that is external to the information-storage circuit for biasing the rectifiers.

68. (Currently amended) The circuit of claim 63 wherein the second voltage is approximately a ground voltage~~or near to ground~~.

69. (Previously presented) The circuit of claim 31 wherein the circuit operates as a random access memory.

70. (Previously presented) The circuit of claim 31 wherein the circuit operates as a read only memory.

71. (Previously presented) The circuit of claim 31 wherein the circuit operates as a one-time-programmable read only memory.

72. – 73. (Cancelled)

74. (Previously presented) The circuit of claim 31 wherein each storage location is a pixel of a display device.

75. (Previously presented) The circuit of claim 74 wherein the nonlinear elements are light emitting.

76. (Currently amended) The circuit of claim 74 wherein the nonlinear elements are light emitting diodes.

77. – 87. (Cancelled)